TMC SPECIFICATION			NO. S1410
REV:			
COMPILED: R. Uzzo	CHECKED:	APPD:	SHEET OF
TITLE:			

PRODUCTION TESTING

(REFERENCE TEST SPECIFICATION)

SMA635376

TMC SPECIFICATION			NO. S1410
REV:			
COMPILED: R. Uzzo	CHECKED:	APPD:	SHEET OF
TITLE:			

1. GENERAL INFORMATION

a) CONTRACTOR - - - - - - - - - - - TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

b) CONTRACT ORDER NUMBER - - - - - DAAB07-81C-1108

c) NOMENCLATURE - - - - - - - - - - SIF CHALLENGE VIDEO ASSEMBLY
P/O AN/TPX - 46
DRAWING NO. SM-D-586748
NSN # 589-00-199-7060

(EQUIPMENTS OF ESTABLISHED DESIGN)

d) SMD 586748 ASSEMBLY
FABRICATED AT: - - - - - - - - - TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

e) SMD 586748 ASSEMBLY - - - - - STOCK NO. REPRESENTED BY
SERIAL NO. _____

f) TESTING LOCATION: - - - - - - TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543

g) TESTING DATE: - - - - - - - - _____

h) TEST SPECIFICATIONS - - - - - SM-A-635376

2. CROSS REFERENCING TABLE FOR SPECIFICATION SMA635376

SPECIFICATION SMA635376 REFERENCE PARAGRAPH NO.	SPECIFICATION DESCRIPTION	PAGE	PARAGRAPH NO.
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3.2.3	SPARE FOUR-INPUT GATE MEASURMENT	6	4.2
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		6	4.6
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		7	5.4

(CONTINUED)

2. CROSS REFERENCING TABLE FOR SPECIFICATION SMA635376

SPECIFICATION SMA635376 REFERENCE PARAGRAPH NO.	SPECIFICATION DESCRIPTION	PAGE	PARAGRAPH NO.
CROSS REFERENCING TABLE FOR SPECIFICATION SMA635376			
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3. PURPOSE

TO ASSURE THAT THE ESTABLISHED, ACCEPTANCE TESTING FOR THE SIF CHALLENGE VIDEO ASSEMBLY IS IN ACCORDANCE WITH TEST REQUIREMENTS, SMA635376.

3.1 TEST EQUIPMENT USED OR EQUIVALENT

a) CON AVIONICS REGULATED LV POWER SUPPLY, MODEL W32-5 TMC ID NO. 1921.

b) E-H RESEARCH LABORATORIES, PULSE GENERATOR MODEL MO139B.
(CALIBRATION EXPIRES 7-6-83, CAL BY RAG SERVICE CALIBRATION)

c) TEKTRONIX OSCILLOSCOPE TYPE 541A.
(CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECTRONICS)

d) HEWLETT PACKARD ELECTRONIC COUNTER MODEL 5245L.
(CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECTRONICS)

e) FLUKE MULTIMETER, MODEL 80208 SERIAL NO. 2801343
(CALIBRATION EXPIRES 7-5-83, CAL BY R & P ELECTRONICS)

(CALIBRATION DATA AVAILABLE ON ALL OF THE ABOVE TEST EQUIPMENT)

3.2 SPECIAL TEST CIRCUIT (ALL UNITS USED TO GENERATE INPUT SIGNALS TO THE TEST CIRCUIT ARE IN CALIBRATION, THE REQUIRED OUTPUT SIGNALS GENERATED BY THE TEST CIRCUIT ARE THE RESULT OF CALIBRATED INPUT SIGNALS.) TMC CONSTRUCTED THE TEST CIRCUIT WHICH IS USED TO GENERATE THE REQUIRED INPUT SIGNALS TO SMD586748

3.3 REFERENCE DATA USED (FIGURE 1-1)

a) SMA635376 (TEST SPECIFICATIONS)

b) SMD586748 (ASSEMBLY DRAWINGS)

c) SME586848 (SCHEMATIC DIAGRAM)

e) TMC TEST CIRCUIT (SCHEMATIC DIAGRAM - FIGURE 1-1) PAGE-14

3.4 TMC-PREPARED TEST SET-UP (SCHEMATIC FIGURE 1-1)

IN ORDER TO PERFORM THE REQUIRED TESTING OF THE SIF CHALLENGE VIDEO ASSEMBLY, TMC HAS PREPARED A TEST SET-UP. THE CIRCUIT THAT ESTABLISHES THE REQUIRED INPUT SIGNALS IS HOUSED IN A .0c ALUM ALY CHASSIS 12 INCHES LENGTH BY 7 INCHES WIDE AND 2 INCHES DEEP. A PRINTED WIRING BOARD WAS CONSTRUCTED TO HOUSE THE CIRCUITS COMPONENTS, FIGURE 1-1 GIVES A SCHEMATIC REPRESENTATION OF THE TEST SET-UP WITH VALUES ADJACENT TO ALL COMPONENT SYMBOLS.

3.4.1 THE FOLLOWING ARE INPUTS DEVELOPED BY TMC'S TEST SET-UP.

INPUT PIN	INPUTS DEVELOPED
17	PULSE: NEGATIVE POLARITY: 1.2MS<PW<1.8MS:
	PRF: 300 PPS.

3.4.1 CON'T.

INPUT PIN	INPUTS DEVELOPED
16	PULSE: NEGATIVE POLARITY: 0.6MS < PW < 0.9MS: POSITION: LEADING EDGE (LE) COINCIDENT WITH THE TRAILING EDGE (TE) OF THE WAVEFORM AT INPUT PIN 17.
18	PULSE: NEGATIVE POLARITY: 0.5uS < PW < 1.5uS PRF: 300 PPS
19	PULSE TRAIN: 0.1uS PERIOD: 0.03uS < PW < 0.07uS
28	PULSE: POSITIVE POLARITY: 0.1uS < PW < 1.0uS POSITION: 350 TO 425 uS AFTER THE LE OF THE PULSE AT INPUT PIN 18.
27	SQUARE WAVE TOGGLE PULSE SQUARE WAVE TOGGLE PULSE CONTROL

3.4.2 SIGNAL REQUIREMENTS

PIN VARIES	HIGH LEVEL (LOGIC"1")
	VOLTAGE DEVELOPED BETWEEN +2.4VDC AND +5.25VDC
PIN VARIES	LOW LEVEL (LOGIC "O")
	VOLTAGE DEVELOPED BETWEEN 0-0.5VDC AND 0+0.5VDC.

3.4.3 POWER REQUIREMENTS

PIN 1 AND 40	VOLTAGE APPLIED +5.±0.25VDC
PIN 2 AND 41	VOLTAGE GROUND RETURN

3.4.4 OUTPUT LOADING

THE FOLLOWING RESISTORS ARE CONNECTED AT THE OUTPUT PINS (SPECIFIED) AND +5±0.25VDC, TO ACCOMPLISH LOADING.

3.4.4 OUTPUT LOADING CON'T (SEE CHART-1 PAGE 13)

OUTPUT PIN	RESISTOR VALUE	LOGIC "0" LOAD	LOGIC "1" LOAD
3	2.7K	1.6 MA	40 uA
4	680 OHM	6.4 MA	160 uA
8	2.7K	1.6 MA	40 uA
14	470 OHM	9.6 MA	240 uA
15	2.7K		200 uA
22	2.7 K	1.6 MA	40 uA
25	1.5K	3.2 MA	80 uA

3.4.5 OUTPUT PIN 15 MEASURES - - - - - - - - - - - - - HIGH LEVEL

4. SPARE FOUR-INPUT GATE TEST
(USING THE TEST SET-UP METRIX) FIGURE 1-1
REFER TO PARAGRAPH 3.2.1.2.1 OF SMA635376 FOR LEVEL DEFINITION.

4.1 CONNECT A JUMPER FROM (LOGIC "1") TERMINAL TO INPUT PIN 10
CONNECT A JUMPER FROM (LOGIC "1") TERMINAL TO INPUT PIN 12
CONNECT A JUMPER FROM (LOGIC "1") TERMINAL TO INPUT PIN 13
CONNECT A JUMPER FROM (LOGIC "1") TERMINAL TO INPUT PIN 21

4.2 OUTPUT PIN 5 MEASURES - - - - - - - - - - - - - LOW LEVEL

4.3 REMOVE THE HIGH LEVEL OR LOGIC "1" JUMPER FROM INPUT PIN 10.
CONNECT A JUMPER FROM "LOGIC O" TERMINAL TO INPUT PIN 10.

4.4 OUTPUT PIN 5 MEASURES - - - - - - - - - - - - - HIGH LEVEL

4.5 REMOVE THE (LOGIC "O") JUMPER FROM INPUT PIN 10.
CONNECT A (LOGIC "1") JUMPER TO INPUT PIN 10.
REMOVE THE (LOGIC "1") JUMPER TO INPUT PIN 12.
CONNECT A (LOGIC "0") JUMPER TO INPUT PIN 12.

4.6 OUTPUT PIN 5 MEASURES - - - - - - - - - - - - - HIGH LEVEL

4.7 REMOVE THE (LOGIC "O") JUMPER TO INPUT PIN 12.
CONNECT A (LOGIC"1") JUMPER TO INPUT PIN 12.
REMOVE THE (LOGIC "1") JUMPER TO INPUT PIN 13.
CONNECT A (LOGIC "O") JUMPER TO INPUT PIN 13.

4.8 OUTPUT PIN 5 MEASURES - - - - - - - - - - - - - HIGH LEVEL

4.9 REMOVE THE "LOGIC O" JUMPER FROM INPUT 13
CONNECT A "LOGIC 1" JUMPER TO INPUT 13
REMOVE THE "LOGIC 1" JUMPER TO INPUT 21
CONNECT A "LOGIC O" JUMPER TO INPUT 21

OUTPUT PIN 5 MEASURES - - - - - - - - - - - - - - - - HIGH LEVEL

4.10 REMOVE ALL JUMPERS FROM INPUT PINS 10, 12, 13 AND 21.

5. A GATE, $\overline{\text{A GATE}}$ TEST
USING THE TEST SET-UP METRIX (FIGURE 1-1)

5.1 CONNECT A JUMPER FROM INPUT PIN 17 TO TERMINAL "B" ON THE TEST SET-UP. TERMINAL "B" IS A NEGATIVE POLARIZED PULSE BETWEEN 1.2MS AND 1.8MS PRF: 300PPS.

5.2 CONNECT A JUMPER FROM INPUT PIN 16 TO TERMINAL "C" ON THE TEST SET-UP. TERMINAL "C" IS A NEGATIVE POLARIZED PULSE BETWEEN 0.6MS AND 0.9MS, POSITIONED WITH THE LEADING EDGE (LE) COINCIDENT WITH THE TRAILING EDGE (TE) OF THE WAVE FORM AT INPUT PIN 17. (USED MODE CHOPPED ON OSCILLOSCOPE 1 MS)

5.3 OUTPUT PIN 6 MEASURES - - - - - - - - - - - - - - - - - - A WAVE FORM
NOTE: USE CHOPPED POSITION ON OSCILLOSCOPE

WHICH GOES HIGH AT THE LE OF THE PULSE AT INPUT PIN 17 AND GOES LOW AT THE LE OF THE PULSE AT INPUT 16

5.4 OUTPUT PIN 8 MEASURES - - - - - - - - - - - - - - - - - - A WAVE FORM WHICH IS THE INVERSE OF THE WAVEFORM AT OUTPUT PIN 6

5.5 REMOVE THE JUMPERS TO INPUT PINS 16 AND 17.

6. SIF INTERLACE, MODE C INTERLACE TEST
(USING THE TEST SET-UP METRIX FIGURE 1-1)

6.1 CONNECT A (LOGIC"1") JUMPER TO INPUT PIN 11.

6.2 CONNECT A (LOGIC "1") JUMPER TO INPUT PIN 26.

6.3 CONNECT A JUMPER FROM INPUT PIN 18 TO TERMINAL "A" ON THE TEST SET-UP. TERMINAL "A" IS A NEGATIVE POLORIZED PULSE BETWEEN 0.5 uS AND 1.5 uS PRF: 300PPS

6.4 OUTPUT PIN 14 MEASURES A SQUARE WAVE WHICH
NOTE: USE ALTERNATE POSITION (-)
INTER. TRIG. ON THE OSCILLOSCOPE 1uS
TOGGLES AT THE LE OF THE PULSE AT INPUT PIN 18

6.5 OUTPUT PIN 7 MEASURES - - - - - - - - - - A SQUARE WAVE
NOTE: USE CHOPPED POSITION
ON OSCILLOSCOPE. 2M SEC SCALE
WHICH IS THE INVERSE OF THE WAVE FORM AT OUTPUT PIN 14

6.6 REMOVE THE "LOGIC 1" JUMPER TO INPUT PIN 11.

6.7 CONNECT A "LOGIC 0" JUMPER TO INPUT PIN 11.

6.8 OUTPUT PIN 14 MEASURES - - - - - - - - - - HIGH LEVEL

6.9 OUTPUT PIN 7 MEASURES - - - - - - - - - - LOW LEVEL

7. RESHAPED SIF CHAL VIDEO TEST

7.1 CONNECT A "LOGIC 1" JUMPER TO INPUT PIN 20.

7.2 CONNECT A "LOGIC 1" JUMPER TO INPUT PIN 24.

7.3 CONNECT A "LOGIC O" JUMPER TO INPUT PIN 23.

7.4 CONNECT A "LOGIC O" JUMPER TO INPUT PIN 27.

7.5 CONNECT A "LOGIC O" JUMPER TO INPUT PIN 36.

7.6 CONNECT A JUMPER FROM INPUT PIN 19 TO TERMINAL "G" ON THE TEST SET-UP. TERMINAL "G" IS A PULSE TRAIN, 0.1uS PERIOD, BETWEEN 0.03uS AND 0.07uS.

7.7 CONNECT A JUMPER FROM INPUT PIN 28 TO TERMINAL "D" ON THE TEST SET-UP. TERMINAL "D" IS A POSITIVE POLARIZED PULSE BETWEEN 0.1uS AND 1.0uS POSITIONED 350 TO 425uS AFTER THE LE OF THE PULSE AT INPUT PIN 18. (USE ADD POSITION ON THE OSCILLOSCOPE 2M SEC - TRIG).

7.8 OUTPUT PIN 4 MEASURES A PULSE PAIR WITH THE FOLLOWING CHARACTERISTICS:

POLARITY Positive

PULSE SPACING 8.0us

PULSE WIDTH ADJUSTABLE BY R1 0.72us TO 0.82us

FINAL ADJUSTMENT 0.88us

POSITION OF SECOND PULSE (USE ADD POSITION OSCILLOSCOPE, 5u SEC) 23±0.5us AFTER LE OF THE PULSE AT INPUT PIN 28

7.9 OUTPUT PIN 3 MEASURES. A PULSE PAIR WHICH IS THE SAME AS OUTPUT PIN 4, EXCEPT THAT THE PULSE PAIR IS INVERTED

(OSCILLOSCOPE POSITION ALT., (-) TRIGGER, 5 uS)

7.10 OUTPUT PIN 25 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS:

POLARITY NEGATIVE

POSITION WITH IN 0.1uS OF THE FIRST PULSE AT OUTPUT PIN 3

PULSE WIDTH 0.7uS TO 1.3uS

(USE ALT POSITION ON THE OSCILLOSCOPE)

7.11 OUTPUT PIN 22 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS.

POLARITY NEGATIVE

POSITION WITH IN 0.1uS OF THE SECOND PULSE AT OUTPUT PIN 3

PULSE WIDTH 0.7uS TO 1.3uS

(USE ADD POSITION ON THE OSCILLOSCOPE)

7.12 REMOVE THE "LOGIC 1" JUMPER FROM INPUT PIN 20.

7.13 CONNECT A "LOGIC 0" JUMPER TO INPUT PIN 20.

7.14 REMOVE THE "LOGIC 0" JUMPER FROM INPUT PIN 36.

7.15 CONNECT A "LOGIC 1" JUMBER TO INPUT PIN 36.

7.16 OUTPUT PIN 4 PULSE PAIR SPACING IS 5uS
(OSCILLOSCOPE "A" ONLY (+) INT TRIGG)

7.17 OUTPUT PIN 3 PULSE PAIR SPACING IS 5uS
(OSCILLOSCOPE "A" ONLY (-) INT TRIGG)

7.18 OUTPUT PIN 25 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS:

POLARITY NEGATIVE

POSITION WITH IN 0.1us OF THE FIRST PULSE AT OUTPUT PIN 3

PULSE WIDTH 0.7us TO 1.3us

(USE ALT POSITION ON THE OSCILLOSCOPE)

7.19 REMOVE THE "LOGIC 1" JUMPER FROM INPUT PIN 36.

7.20 CONNECT A "LOGIC O" JUMPER TO INPUT PIN 36.

7.21 REMOVE THE"LOGIC O" JUMPER FROM INPUT PIN 27.

7.22 CONNECT A"LOGIC 1" JUMPER TO INPUT PIN 27.

7.23 OUTPUT PIN 4 PULSE PAIR SPACING IS 3 us
(OSCILLOSCOPE "A" ONLY (+) INT TRIGG)

7.24 OUTPUT PIN 3 PULSE PAIR SPACING IS 3 us
(OSCILLOSCOPE "A" ONLY (-) INT TRIGG)

7.25 OUTPUT PIN 25 MEASURES A PULSE WITH THE FOLLOWING CHARACTERISTICS:

POLARITY NEGATIVE

POSITION WITH IN 0.1 us OF THE FIRST PULSE AT OUTPUT PIN 3

PULSE WIDTH 0.7us TO 1.3us (USE ALT POSITION)

7.26 REMOVE THE "LOGIC 1" JUMPER FROM INPUT PIN 27.

7.27 CONNECT A JUMPER FROM INPUT PIN 27 TO TERMINAL "I" ON THE T T SET-UP. TERMINAL "I" IS A SQUARE WAVE WHICH TOGGLES AT THE E OF THE PULSE AT INPUT PIN 18. (USE ALT POSITION)

7.28 CONNECT A JUMPER FROM INPUT PIN"14" TO TERMINAL "H" PIN 14 WILL GO TO A HIGH LEVEL.

7.29 OUTPUT PIN 4 MEASURES - - - - - - - - - - - - A PULSE PAIR WITH 3us SPACING "A" ONLY (OSCILLOSCOPE (+) TRIGGER)

7.30 REMOVE THE "LOGIC 1" JUMPER FROM INPUT PIN 26.

7.31 CONNECT A "LOGIC O" JUMPER TO INPUT PIN 26.

7.32 OUTPUT PIN 14 MEASURES - - - - - - - - - - - - - LOW LEVEL

7.33 OUTPUT PIN 4 MEASURES - - - - - - - - - - - - - A PLUSE PAIR WITH 21 uS SPACING

(OSCILLOSCOPE "A" ONLY, INTER TRIGG (+) 5u Sec)

END OF TEST

ALL TEST REQUIREMENTS FOR THE SIF CHALLENGE VIDEO ASSEMBLY SMD586748 HAVE BEEN COMPLIED WITH, IN ACCORDANCE WITH "TEST REQUIREMENTS SIF CHALLENGE VIDEO ASSEMBLY SMA635376"

ALL TEST PROCEDURES SPECIFIED IN THIS TEXT WILL BE IMPLEMENTED DURING TESTING OF ALL SMD586748 ASSEMBLIES.

DATE TEST WAS PERFORMED _____

TESTERS SIGNATURE _____ SERIAL NO._____

WITNESSED BY:

GOVERNMENT REPRESENTIVE_____

DATE_____