

TMC SPECIFICATION

NO. S1413

REV:

COMPILED: R. UZZO

CHECKED:

APPD:

SHEET

OF

TITLE: FIRST ARTICLE APPROVAL - CONTRACTOR TESTING

SERIAL NO.

FIRST ARTICLE APPROVAL

CONTRACTOR TESTING

(SMA587233)

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1. GENERAL INFORMATION

- a) CONTRACTOR - - - - - TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543
- b) CONTRACT ORDER NUMBER - - DAAB07-81C-1131
ITEM 0004AC FOR ITEM 0003
- c) NOMENCLATURE - - - - - REPLY DISCRIMINATOR ASSEMBLY
P/O AN/TPX - 46 (V)
DRAWING NO. SM-D-586701
NSN # 5895-00-199-7054

(EQUIPMENTS OF ESTABLISHED DESIGN)

- d) FIRST ARTICLE FABRICATED AT:
TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543
- e) FIRST ARTICLE - - - - - STOCK NO. REPRESENTED BY
SERIAL NO'S 001 AND 002
- f) FIRST ARTICLE TESTING LO-
CATION: - - - - - TECHNICAL MATERIEL CORPORATION
700 FENIMORE ROAD
MAMARONECK, NEW YORK 10543
- g) FIRST ARTICLE TESTING DATE: _____
- h) FIRST ARTICLE TEST SPE-
CIFICATIONS - - - - - SM-A-587233
- i) AMENDMENT MODIFICATION
P00002 (CHANGE NOTICE NO.
58598
- j) THIS IS TO CERTIFY THAT THE FIRST ARTICLE WAS MANUFACTURED
AT THE TECHNICAL MATERIEL CORPORATION FACILITY 700 FENIMORE
ROAD, MAMARONECK, NEW YORK 10543. THE PRODUCTION LOT WILL
BE MANUFACTURED AND TESTED IN THE IDENTICAL MANNER AS THE
FIRST ARTICLE.

Eugene J. Hofmann, President

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2. CROSS REFERENCING TABLE FOR SPECIFICATION SMA587233

SPECIFICATION SMA587233 REFERENCE PARAGRAPH NO.	SPECIFICATION DESCRIPTION	PAGE	PARAGRAPH NO.
3.2.1.1	POWER REQUIREMENTS	4	3.4.2
3.2.1.2	SIGNAL REQUIREMENTS	4	3.4.1
3.2.1.2.3	LOAD REQUIREMENTS	4	3.4.3
3.2.1.2.6	TOLERANCES	4	3.4.4
3.2.1.2.8	ADJUSTMENT PROCEDURES	6	4
3.2.2.2	TEST NO 1 OUTPUTS	6	6
3.2.3.2	TEST NO 2 OUTPUTS	7	8
3.2.4.2	TEST NO 3 OUTPUTS	7	10
3.2.5.2	TEST NO 4 OUTPUTS	7	12
3.2.6.2	TEST NO 5 OUTPUTS	8	14
3.2.7.2	TEST NO 6 OUTPUTS	8	16
3.2.8.2	TEST NO 7 OUTPUTS	8	18
3.2.9	TEST NO 8	8	20
3.2.10	TEST NO 9	9	22

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3. PURPOSE

TO ASSURE THAT THE ESTABLISHED, ACCEPTANCE TESTING FOR THE REPLY DISCRIMINATOR ASSEMBLY IS IN ACCORDANCE WITH TEST REQUIREMENTS, SMA587233.

3.1 TEST EQUIPMENT USED OR EQUIVALENT

- a) CON AVIONICS REGULATED LV POWER SUPPLY, MODEL W32-5 TMC ID NO. 1921.
- b) E-H RESEARCH LABORATORIES, PULSE GENERATOR MODEL MO139B. (CALIBRATION EXPIRES 7-6-83, CAL BY RAG CAL SERVICE)
- c) TEKTRONIX OSCILLOSCOPE TYPE 541A. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECT.)
- d) HEWLETT PACKARD ELECTRONIC COUNTER MODEL 524L. (CALIBRATION EXPIRES 5-19-83, CAL BY R & P ELECT.)
- e) FLUKE MULTIMETER, MODEL 80208 SERIAL NO. 2801343. (CALIBRATION EXPIRES 7-5-83, CAL BY R & P ELECT.)

- 3.2 SPECIAL TEST CIRCUIT (ALL UNITS USED TO GENERATE INPUT SIGNALS TO THE TEST CIRCUIT ARE IN CALIBRATION, THE REQUIRED OUTPUT SIGNALS GENERATED BY THE TEST CIRCUIT ARE THE RESULT OF CALIBRATED INPUT SIGNALS.) TMC CONSTRUCTED THE TEST CIRCUIT, IN ORDER TO GENERATE THE REQUIRED INPUT SIGNALS TO THE SMD586701 ASSEMBLY.

(SEE FIGURE 1-1)

3.3 REFERENCE DATA USED

- a) SMA587233 (TEST SPECIFICATIONS)
- b) CHANGE NOTICE NO. 58468 (3 SHEETS)
- c) SMD586701 (ASSEMBLY DRAWINGS)
- d) SME586801 (SCHEMATIC DIAGRAM)
- e) TMC TEST CIRCUIT (SCHEMATIC DIAGRAM - FIGURE 1-1 PAGE

3.4 TMC-PREPARED TEST CIRCUIT (SCHEMATIC FIGURE 1-1)

TMC HAS PREPARED A TEST CIRCUIT TO GENERATE THE REQUIRED INPUT SIGNALS NECESSARY IN TESTING THE REPLY DISCRIMINATOR ASSEMBLY. THIS TEST CIRCUIT IS HOUSED IN A .063 ALUM ALY CHASSIS 12 INCHES LONG BY 7 INCHES WIDE AND 2 INCHES DEEP. A PRINTED WIRING BOARD WAS CONSTRUCTED TO HOUSE THE CIRCUITS COMPONENTS, FIGURE 1-1 GIVES A SCHEMATIC REPRESENTATION OF THE TEST CIRCUIT. ALL COMPONENT VALUES USED IN THE TEST CIRCUIT ARE CALLED OUT IN THE SCHEMATIC DIAGRAM (FIGURE 1-1), AND ARE FOUND ADJACENT TO ALL COMPONENT SYMBOLS.

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3.4.1 SIGNAL REQUIREMENTS

PIN VARIES HIGH LEVEL (LOGIC "1")
VOLTAGE DEVELOPED BETWEEN +2.4VDC AND
+5.05VDC.

PIN VARIES LOW LEVEL (LOGIC "0")
VOLTAGE DEVELOPED BETWEEN 0 - OVDC AND
0 + 0.8VDC.

3.4.2 POWER REQUIREMENTS

PIN 1 AND 40 VOLTAGE APPLIED +5 \pm .05VDC
PIN 2,
41 AND 16 VOLTAGE GROUND RETURN

3.4.3 OUTPUT LOADING

THE FOLLOWING RESISTORS ARE CONNECTED AT THE OUTPUT PINS
(SPECIFIED) AND +5 \pm .05VDC TO ACCOMPLISH LOADING.

OUTPUT PIN	RESISTOR VALUE	LOGIC "0" SOURCE CURRENT	LOGIC "1" SINK CURRENT
4	270 OHM	16 mA	400 μ A
18	270 OHM	16 mA	400 μ A
25	470 OHM	9.6 mA	240 μ A
32	100 OHM	48 mA	1200 μ A
38	100 OHM	44.8 mA	1120 μ A

3.4.4 ALL TOLERANCES ARE \pm 10% UNLESS OTHERWISE SPECIFIED.

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3.4.5 THE FOLLOWING ARE INPUTS DEVELOPED BY TMC'S TEST CIRCUIT

<u>INPUT PIN</u>	<u>DESCRIPTION</u>
19	CONTINUOUS PULSE TRAIN, POSITIVE, 1.1 us PULSE WIDTH (INHIBIT)
28	CONTINUOUS PULSE TRAIN, POSITIVE .8 us PULSE WIDTH 2 us AFTER THE (TE) OF THE INHIBIT PULSE. (SHIFT)
30	CONTINUOUS PULSE TRAIN, NEGATIVE 75 ns + 25 ns PULSE WIDTH, 750 ns + 150 ns AFTER THE (TE) OF THE INHIBIT PULSE (READ) STROBE
29	CONTINUOUS PULSE TRAIN, NEGATIVE 100 ns PULSE WIDTH, .3 us AFTER THE (TE) OF THE INHIBIT PULSE (3 DECODE)
33	<u>NEGATIVE PULSE .1 TO 4 us PULSE WIDTH DECODE REPLY</u>
34 or 36	NEGATIVE PULSE 4.12 us PULSE WIDTH
23	NEGATIVE O/E SENSE PULSE
23	POSITIVE O/E SENSE PULSE

3.4.6 J1-6 CONNECTOR

A CONNECTION TO TERMINAL J1-6 IS NECESSARY TO SYNCHRONIZE ALL OF THE DEVELOPED INPUT PULSES. J1-6 IS ROUTED TO THE OSCILLOSCOPE TRIGGER INPUT VIA THE TMC TEST CIRCUIT.
(SEE SCHEMATIC DIAGRAM FIGURE 1-1.)

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4. ADJUSTMENT PROCEDURE

CONNECT PIN 26 TO LOGIC "1"

CONNECT PIN 19 TO TERMINAL "E"

CONNECT PIN 30 TO TERMINAL "A"

4.1 MONITOR J1-2 AND OBTAIN A PULSE WIDTH OF 2.8 us BY ADJUSTING R1.

4.2 MONITOR J1-2 AND OBTAIN A PULSE WIDTH OF 3.5 us BY ADJUSTING R1.

4.3 MONITOR J1-2 AND SET R1 FOR 3 us.

4.4 MONITOR J2-5 AND OBTAIN A PULSE WIDTH OF 2.8 us BY ADJUSTING R2.

4.5 MONITOR J2-5 AND OBTAIN A PULSE WIDTH OF 3.5 us BY ADJUSTING R2.

4.6 MONITOR J2-5 AND SET R2 FOR 3 us.

REMOVE ALL JUMPER CONNECTIONS

5. TEST NO.1 INPUTS

5.1 CONNECT PIN 33 TO TERMINAL B5.2 CONNECT PIN 28 TO TERMINAL C5.3 CONNECT PIN 30 TO TERMINAL A5.4 CONNECT PIN 29 TO TERMINAL D5.5 CONNECT PIN 19 TO TERMINAL E5.6 CONNECT PIN 34 TO TERMINAL F5.7 CONNECT PIN 36 TO LOGIC "1" TERMINAL5.8 CONNECT PIN 35 TO LOGIC "1" TERMINAL5.9 CONNECT PIN 37 TO LOGIC "1" TERMINAL5.10 CONNECT PIN 26 TO LOGIC "1" TERMINAL

5.11 TIME SWITCH SET TO POSITION 1.

5.12 GATE SWITCH SET TO POSITION 1.

6. TEST NO. 1 OUTPUTS

MONITOR PIN 4 (REPLY) LOW AT TIME 5.HIGH AT TIME 8.

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7. TEST NO.2 INPUTS

7.1 TIME SWITCH SET TO POSITION 2

7.2 CONNECT PIN 23 TO TERMINAL H

8. TEST NO.2 OUTPUTS

MONITOR PIN 4 (REPLY) LOW AT TIMES 5 AND 8HIGH AT TIMS 11

9. TEST NO.3 INPUTS

9.1 REMOVE PIN 23 FROM TERMINAL H9.2 CONNECT PIN 23 TO TERMINAL G

9.3 GATE SWITCH SET TO POSITION 2

10. TEST NO.3 OUTPUTS

MONITOR PIN 4 (REPLY) LOW AT TIMES 8 AND 11HIGH AT TIME 14

11. TEST NO.4 INPUTS

TIME SWITCH SET TO POSITION 1

12. TEST NO.4 OUTPUTS

MONITOR PIN 4 LOW AT TIME 8HIGH AT TIME 11

13. TEST NO. 5 INPUTS

REMOVE PIN 26 FROM LOGIC 1 TERMINALCONNECT PIN 26 TO LOGIC 0 TERMINAL

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14. TEST NO.5 OUTPUTSMONITOR TEST POINT J1-6 HIGH15. TEST NO.6 INPUTS

TIME SWITCH SET TO POSITION 2

GATE SWITCH SET TO POSITION 1

REMOVE PIN 23 FROM TERMINAL GCONNECT PIN 23 TO LOGIC "0"REMOVE PIN 26 FROM A LOGIC "0" TERMINALCONNECT PIN 26 TO A LOGIC "1" TERMINAL16. TEST NO.6 OUTPUTSMONITOR PIN 18 LOW AT TIMES 7 AND 1017. TEST NO.7 INPUTS

GATE SWITCH SET TO POSITION 2

REMOVE PIN 23 FROM LOGIC "0" TERMINALCONNECT PIN 23 TO LOGIC 1 TERMINAL18. TEST NO.7 OUTPUTSMONITOR PIN 18 HIGH AT TIMES 10 & 1319. REMOVE ALL JUMPER CONNECTS20. TEST NO.8

20.1 CONNECT LOGIC 1 TO PIN 31

20.2 MONITOR PIN 32 LOW LEVEL

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20.3 CONNECT LOGIC 0 TO PIN 31

20.4 MONITOR PIN 32 HIGH LEVEL

20.5 CONNECT LOGIC 1 TO PIN 30

20.6 MONITOR PIN 25 LOW LEVEL

20.7 CONNECT LOGIC "0" TO PIN 30

20.8 MONITOR PIN 25 HIGH LEVEL

21. REMOVE ALL JUMPER PINS

22. TEST NO.9

CONNECT THE FOLLOWING PINS TO LOGIC "1" 33, 34, 35, 36 AND 37

22.1 MONITOR PIN 38 HIGH LEVEL

22.2 REMOVE PIN 33 FROM THE LOGIC "1" TERMINAL

CONNECT PIN 33 TO A LOGIC "0" TERMINAL

22.3 MONITOR PIN 38 LOW LEVEL

22.4 REMOVE PIN 34 FROM THE LOGIC "1" TERMINAL

CONNECT PIN 34 TO A LOGIC "0" TERMINAL

REMOVE PIN 33 FROM A LOGIC "0" TERMINAL

CONNECT PIN 33 TO A LOGIC "1" TERMINAL

22.5 MONITOR PIN 38 HIGH LEVEL

22.6 REMOVE PIN 34 FROM LOGIC "0" TERMINAL

CONNECT PIN 34 TO LOGIC "1" TERMINAL

REMOVE PIN 35 FROM LOGIC "1" TERMINAL

CONNECT PIN 35 TO LOGIC "0" TERMINAL

22.7 MONITOR PIN 38 HIGH LEVEL

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- 22.8 REMOVE PIN 36 FROM A LOGIC "1" TERMINAL
CONNECT PIN 36 TO A LOGIC "0" TERMINAL
REMOVE PIN 35 FROM LOGIC "0" TERMINAL
CONNECT PIN 35 TO LOGIC "1" TERMINAL
- 22.9 MONITOR PIN 38 HIGH LEVEL
- 22.10 REMOVE PIN 36 FROM A LOGIC "0" TERMINAL
CONNECT PIN 36 TO A LOGIC "1" TERMINAL
REMOVE PIN 37 FROM A LOGIC "1" TERMINAL
CONNECT PIN 37 TO A LOGIC "0" TERMINAL
- 22.11 MONITOR PIN 38 LOW LEVEL

END OF TEST

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CALCULATIONS FOR LOADING

OUTPUT PIN	SINK CURRENT LOGIC "1"	SOURCE CURRENT LOGIC "0"	CALCULATIONS USING LOGIC "1" AS REFERENCE	REQUIRED RESISTANCE + 10% FROM CALCULATED RESULTS
32	48 mA	1200uA	$5V - .5V = 4.5V$ $\frac{4.5V}{48 \text{ mA}} = 93$	100 OHM
38	44.8 mA	1120uA	$5V - .5V = 4.5V$ $\frac{4.5V}{44.8 \text{ mA}} = 102$	100 OHM
18 AND 4	16 mA	400uA	$5V - .5V = 4.5V$ $\frac{4.5V}{16 \text{ mA}} = 281$	270 OHM
25	9.6 mA	240uA	$5V - .5V - 4.5$ $\frac{4.5V}{9.6 \text{ mA}} = 468$	470 OHM

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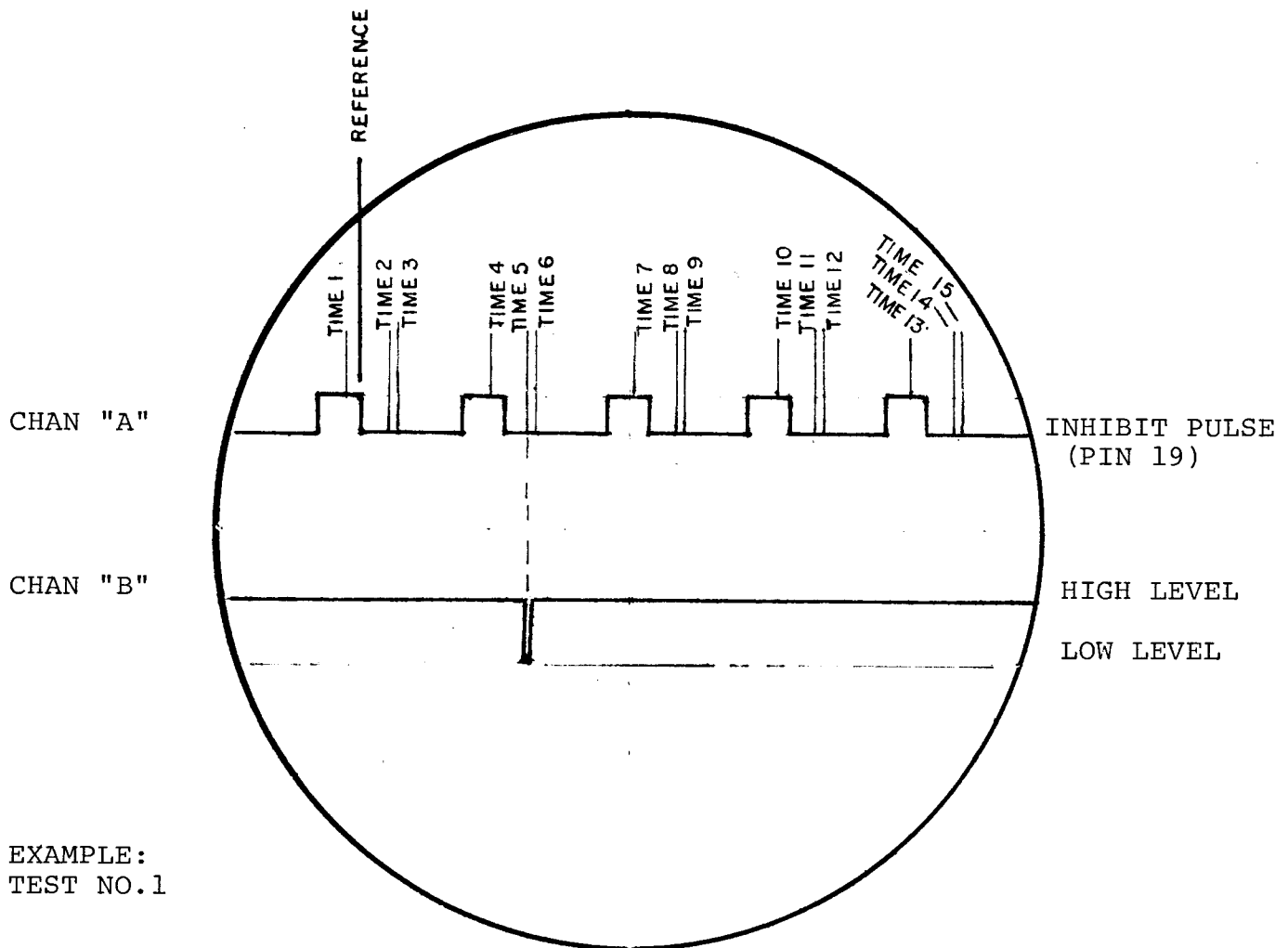
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EXAMPLE:
TEST NO.1

NOTE:

THE INHIBIT PULSE AT PIN 19 IS USED FOR TIME REFERENCING. ALL READINGS ARE MONITORED WITH RELATION TO THE INHIBIT PULSE.

TO SYNC (OSCILLOSCOPE)

TO J1-6

+5V

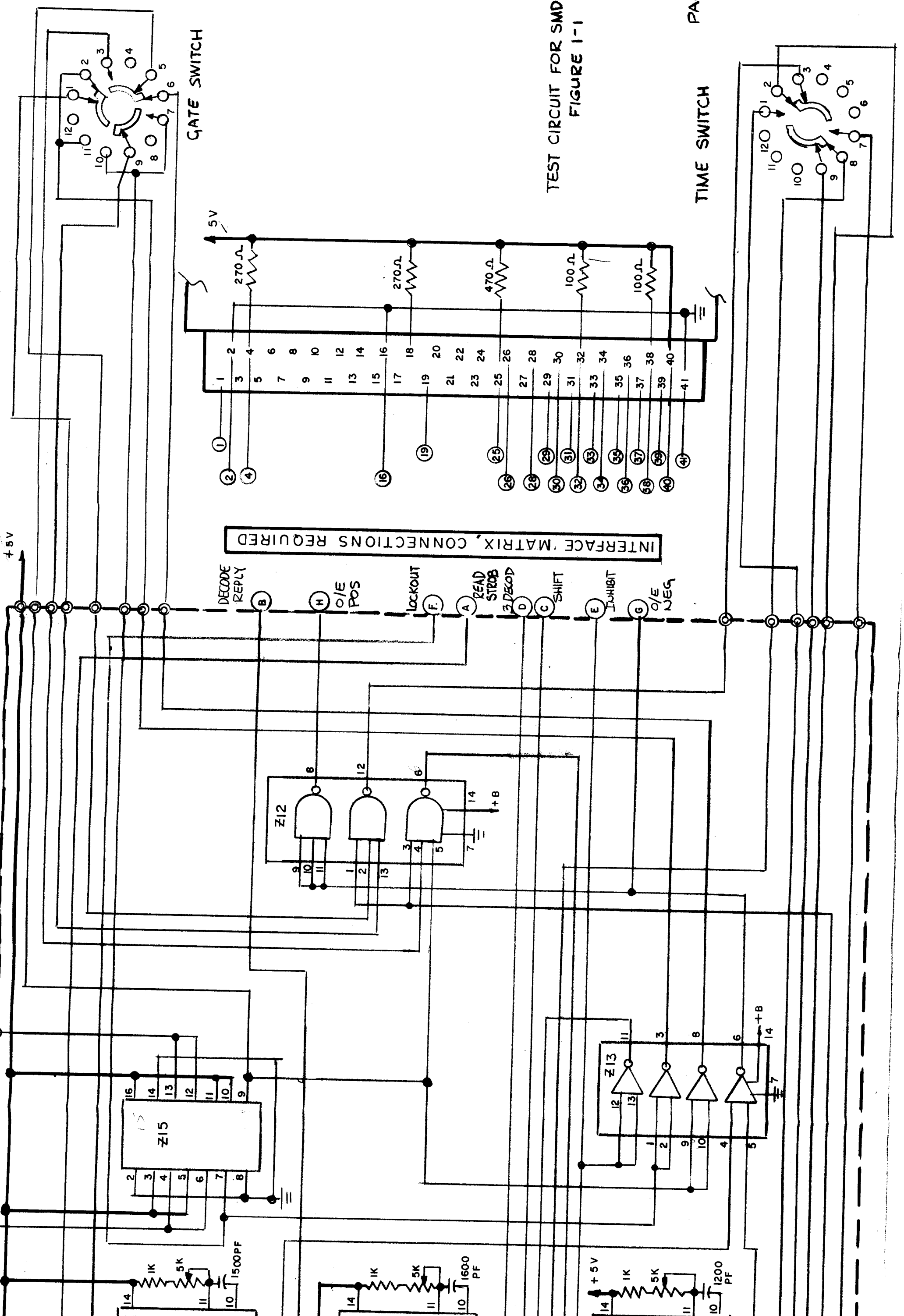
GATE SWITCH

TIME SWITCH

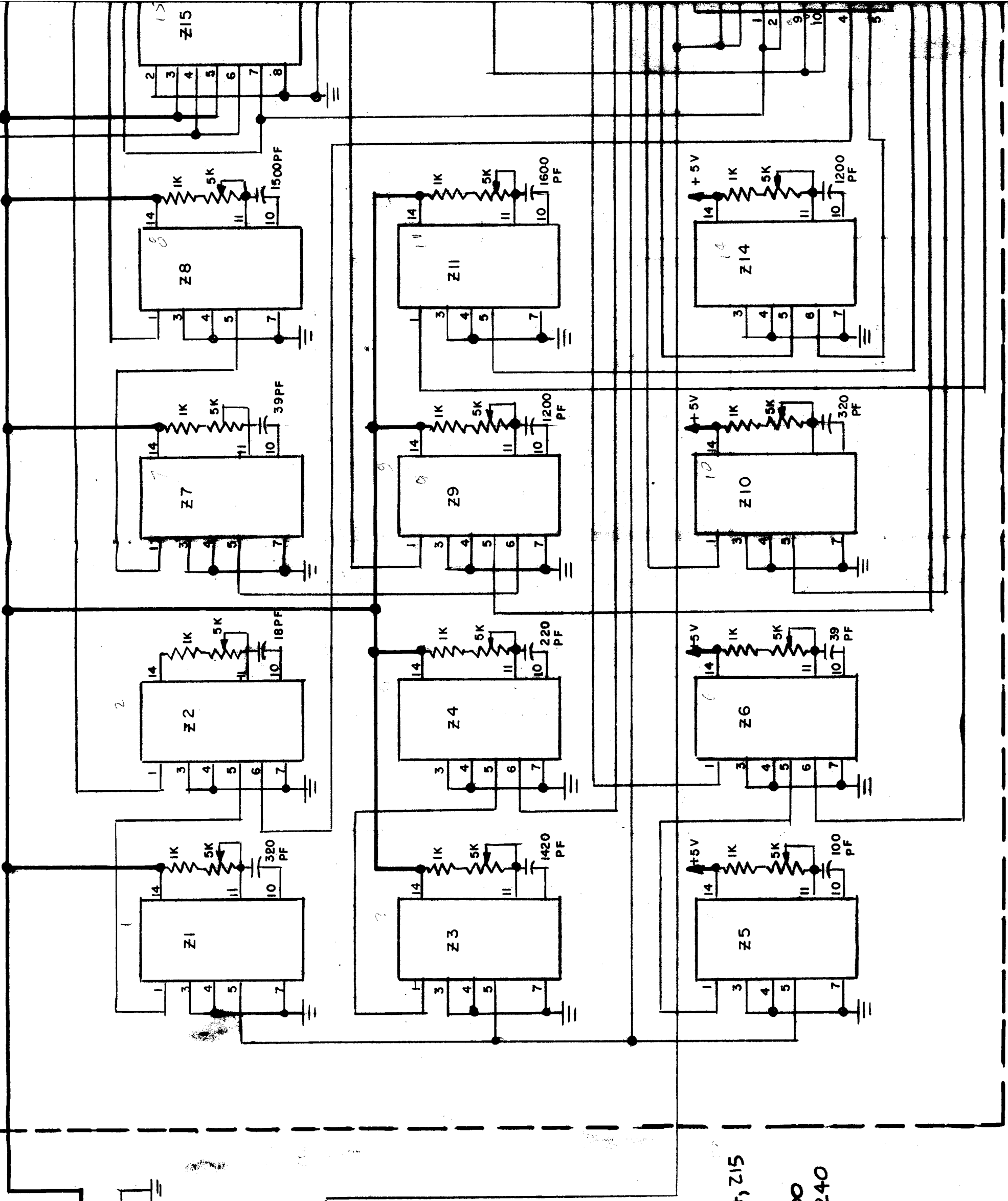
INTERFACE MATRIX, CONNECTIONS REQUIRED

A READ STROB
 B DECODE REPLY
 C SHIFT
 D 3 DECOD
 E INHIBIT
 F LOCKOUT
 G O/E NEG
 H O/E POS

TEST CIRCUIT FOR SMD586701
FIGURE 1-1



TO J1-6



POWER
SUPPLY
5V ± 0.05

GEN
243.9
KHZ

Z1 THRU 11, Z14, Z15
ARE MC74121
Z12 IS SN7400
Z13 IS SN74240

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ALL TEST REQUIREMENTS FOR THE POST REPLY DISCRIMINATOR ASSEMBLY SMD586701 HAVE BEEN COMPLIED WITH, IN ACCORDANCE WITH "TEST REQUIREMENTS SMA587233."

ALL TEST PROCEDURES SPECIFIED IN THIS TEXT WILL BE IMPLEMENTED DURING TESTING OF ALL SMD586701 ASSEMBLIES.

DATE TEST WAS PERFORMED _____

TESTERS SIGNATURE _____ SERIAL NO. _____

WITNESSED BY

GOVERNMENT REPRESENTATIVE _____

DATE _____