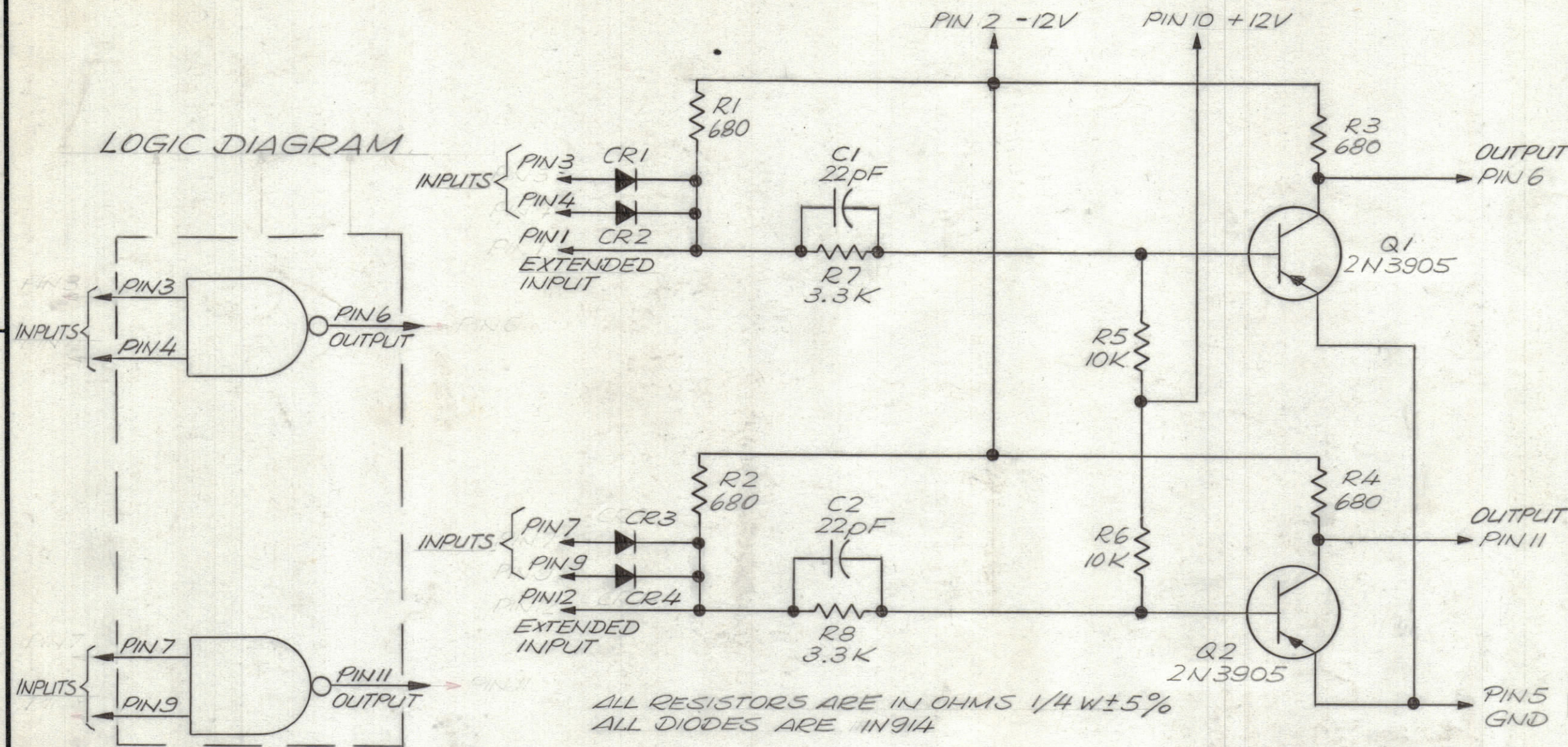


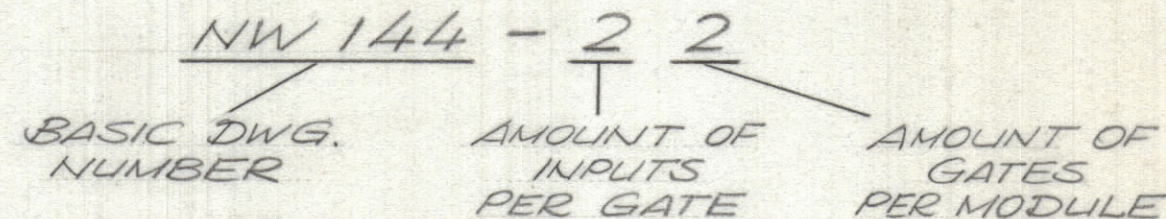
NW 144-22

SCHEMATIC DIAGRAM



REVISIONS						
ZONE	LTR	DESCRIPTION	DATE	E.M.N.NO	DRAFT	CHKD
	X	EXP. RELEASE	9/26/69			
	X1	REV. & UPDATED	11/13/69			
	X2	12 VOLT LOGIC TO ELEC. SPEC. ADD	11/16/69			
	Ø	ORIGINAL RELEASE FOR PRODUCTION	4/24/70			

TMC PART NUMBER SHALL APPEAR IN THE FOLLOWING FORM:



ELECTRICAL SPECIFICATIONS

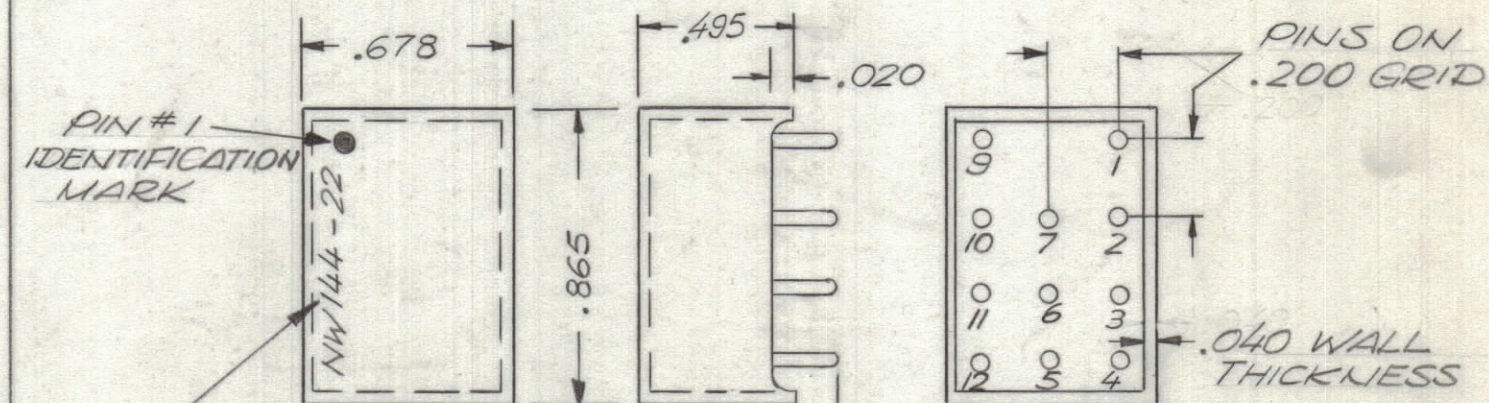
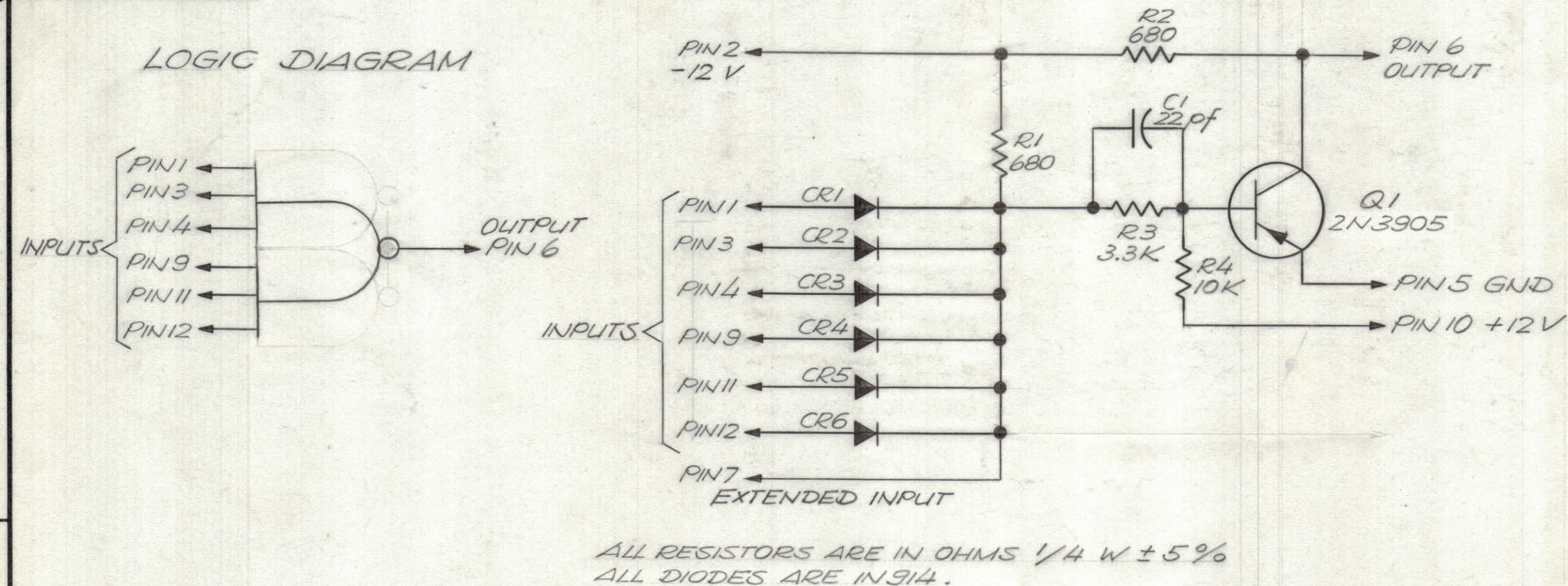
12 VOLT LOGIC
PIN # 5 GND
PIN # 2 -12V
PIN # 10 +12V
OPERATING TEMPERATURE 0°C TO + 75°C
SWITCHING CHARACTERISTICS
EACH INPUT MIN. VOLTAGE - -6.0 VDC
EACH OUTPUT MIN. VOLTAGE -10.0 VDC
INPUT $T_r = .08 \mu\text{sec}$ $T_f = .12 \mu\text{sec}$
OUTPUT $T_r = .08 \mu\text{sec}$ $T_f = .12 \mu\text{sec}$

MECHANICAL SPECIFICATIONS

POTTING COMPOUND: EPOTEC 509
CASE MATERIAL: DIALYL PHTHALATE
POLARIZING PIN: PIN # 8

NW 144-61

SCHEMATIC DIAGRAM



MARKING TO BE APPROX. 1/8 HIGH WHITE GOTHIC EPOXY

MARK AS REQ.:
NW 144 - 22
NW 144 - 61

NOTE:
PINS ARE EXTRUDED COMPONENT LEADS. (DO NOT USE TRANSISTOR LEADS FOR MTG. PINS.)

QTY. REQ.	ITEM	PART NO.	DESCRIPTION	SYMBOL
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LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES	FINAL APPROVAL <i>S. De Marco</i> MECH. DES. DATE 2/24/70
TOLERANCES ON	ELECT. DES. DATE
DECIMALS .X ± .05 .XX ± .01 .XXX ± .005	CHECKED <i>M. Quich</i> DATE 1/24/69
FRACTIONS ± 1/64 ANGLES ± 0° -30'	DRAWN <i>G. Evangelist</i> DATE 4.8.69

THE TECHNICAL MATERIEL CORP.
MAMARONECK, NEW YORK

NETWORK, DIGITAL
NAND GATE AMPLIFIER

QTY / UNIT	MODEL USED ON	ASS'Y NO.
	DDRR 10M, K	
APPLICATION		
CODE		

MATERIAL	SIZE	CODE IDENT. NO.	DWG NO.	ISSUE
FINISH	C	82679	NW 144	Ø
	SCALE		SHEET	OF

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